CLAIMS

What is claimed is:

1. A method of power sequence protection for a level shifter comprising the steps of:

(a) placing the level shifter in a pre-selected state if an input voltage supply for an input signal is not powered on before an output voltage supply for an output signal is powered on; and

(b) releasing the level shifter from the pre-selected state to follow transitions of an input signal when the input voltage supply is powered on.

2. The method of Claim 1 wherein step (a) comprises connecting a common voltage rail to an output signal port or an inverted output signal port of the level shifter.

3. The method of Claim 2 wherein step (b) comprises presenting a high impedance to the output signal port or the inverted output signal port of the level shifter.

4. A power sequence protection circuit comprising:

a latch electrically coupled to an input voltage supply and an output voltage supply; and

a switch electrically coupled to the latch wherein the switch has a first state for holding a level shifter in a pre-selected state if the output voltage supply is powered on when the input voltage supply is not powered

on and a second state for releasing the level shifter from the pre-selected state to follow transitions of an input signal if the input voltage supply is powered on.

5. The power sequence protection circuit of Claim 4 wherein the switch connects a common voltage rail to an output signal port or an inverted output signal port of the level shifter in the first state.

6. The power sequence protection circuit of Claim 5 wherein the switch presents a high impedance to the output signal port or the inverted output signal port of the level shifter in the second state.

7. The power sequence protection circuit of Claim 4 further comprising the level shifter.

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